



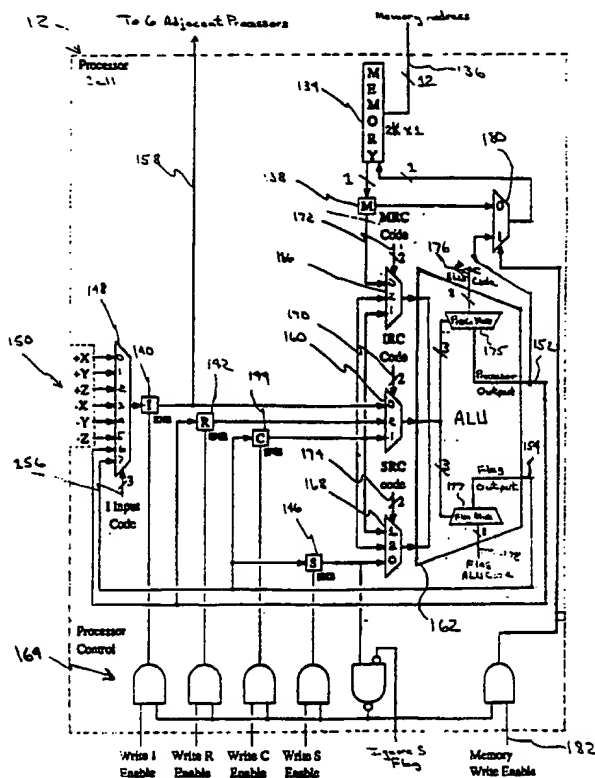
## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

|   |   |   |
|---|---|---|
| (51) International Patent Classification 5 :<br><b>G06F 15/80</b>   | <b>A1</b>   | (11) International Publication Number: <b>WO 91/19269</b><br>(43) International Publication Date: 12 December 1991 (12.12.91) |
| <p>(21) International Application Number: PCT/US91/03347</p> <p>(22) International Filing Date: 14 May 1991 (14.05.91)</p> <p>(30) Priority data:<br/>530,027 29 May 1990 (29.05.90) US</p> <p>(71) Applicant: WAVETRACER, INC. [US/US]; 289 Great Road, Acton, MA 01720 (US).</p> <p>(72) Inventors: JACKSON, James, H. ; 119 Penwood Drive, Cary, NC 27511 (US). LEE, Ming-Chih ; 126 Karen Court, Cary, NC 27511 (US). LAFOREST, Mark, R. ; 32 Clements Road, Waltham, MA 02154 (US). FIORENTINO, Richard, D. ; 43 Aaron Way, Carlisle, MA 01741 (US).</p> | <p>(74) Agents: GAGNEBIN, Charles, L., III et al.; Weingarten, Schurgin, Gagnebin &amp; Hayes, Ten Post Office Square, Boston, MA 02109 (US).</p> <p>(81) Designated States: AT (European patent), AU, BE (European patent), CA, CH (European patent), DE (European patent), DK (European patent), ES (European patent), FR (European patent), GB (European patent), GR (European patent), IT (European patent), JP, LU (European patent), NL (European patent), SE (European patent).</p> <p><b>Published</b><br/>With international search report.<br/>With amended claims.</p> |   |

(54) Title: MULTI-DIMENSIONAL PROCESSOR SYSTEM AND PROCESSOR ARRAY WITH MASSIVELY PARALLEL INPUT/OUTPUT

## (57) Abstract

A multi-dimensional processor system and processor array (10) with massively parallel input/output includes a processor array (10) having a plurality of processor cells (12) interconnected to form an N-dimensional array. The preferred embodiment includes at least one input/output device (118) coupled to one data signal port of selected processor cells each having 2N dimensionally adjacent processor cells, and connected to a surplus data signal port of a second group of processor cells each having fewer than 2N dimensionally adjacent processor cells, for providing massively parallel input/output between the multi-dimensional processor array and the input/output device. The processor system also includes a front end processor (102) for providing processor array instructions in response to application programs running on the front end processor. A processor cell controller (104), responsive to the processor array commands, broadcasts a sequence of processor cell instructions to all of the processor cells of the multi-dimensional processor array.



**FOR THE PURPOSES OF INFORMATION ONLY**

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

|    |                          |    |  |    |                          |
|----|--------------------------|----|--|----|--------------------------|
| AT | Austria                  | ES | Spain                                    | MG | Madagascar               |
| AU | Australia                | FI | Finland                                  | ML | Mali                     |
| BB | Barbados                 | FR | France                                   | MN | Mongolia                 |
| BE | Belgium                  | GA | Gabon                                    | MR | Mauritania               |
| BF | Burkina Faso             | GB | United Kingdom                           | MW | Malawi                   |
| BG | Bulgaria                 | GN | Guinea                                   | NL | Netherlands              |
| BJ | Benin                    | GR | Greece                                   | NO | Norway                   |
| BR | Brazil                   | HU | Hungary                                  | PL | Poland                   |
| CA | Canada                   | IT | Italy                                    | RO | Romania                  |
| CF | Central African Republic | JP | Japan                                    | SD | Sudan                    |
| CG | Congo                    | KP | Democratic People's Republic<br>of Korea | SE | Sweden                   |
| CH | Switzerland              | KR | Republic of Korea                        | SN | Senegal                  |
| CI | Côte d'Ivoire            | LI | Liechtenstein                            | SU | Soviet Union             |
| CM | Cameroon                 | LK | Sri Lanka                                | TD | Chad                     |
| CS | Czechoslovakia           | LU | Luxembourg                               | TG | Togo                     |
| DE | Germany                  | MC | Monaco                                   | US | United States of America |
| DK | Denmark                  |    |  |    |                          |

- 1 -

MULTI-DIMENSIONAL PROCESSOR SYSTEM AND PROCESSOR ARRAY  
WITH MASSIVELY PARALLEL INPUT/OUTPUT

## FIELD OF THE INVENTION

This invention relates to parallel processors and more particularly, to a multi-dimensional processor system.

5 BACKGROUND OF THE INVENTION

Natural phenomena such as electric and magnetic fields, fluid flows, sound waves, and heat flow are, at any given moment in time, represented as spatially distributed data in a three dimensional manner by a set of numbers whose indices represent spacial positioning along three mutually orthogonal axes. On occasion, a fourth dimension, namely time, must also be considered. To date, scientists and other computer users wishing to solve partial differential equations that involve spatially distributed data such as Poisson's or Maxwell's equations have had limited data processing capabilities because prior art processor systems and processor arrays have been limited to two-dimensional architectures.

Prior art attempts at solving three-dimensional equations utilizing purely one- or two-dimensional arrays have yielded processing systems requiring a large amount of "processor overhead" to calculate an index or address pointer to the second or third dimension of the spatial data which must be stored in memory and not in a processor. For example, in a traditional single processor computer, computing the Z or third dimension index requires up to three multiplications and two addition steps. On a two-dimensional computer, although the X and Y axes are directly accessible, the Z pointer must be calculated which still requires up to one multiplication and one addition.

- 2 -

Prior art attempts at dealing with three-dimensional data also include the utilization of an interconnection arrangement such as that disclosed in U.S. Patent No. 4,814,973 in which routers may be instructed to switch data between processor cells in a fashion that mimics the behavior of a three-dimensional processor array. Routers, however, require a large amount of processor overhead to move data between the various processor cells. In addition, supporting control circuitry is required to perform the switching function. System throughput or bandwidth is significantly compromised by the router overhead, and system cost and reliability are compromised due to the necessity of including the routers and associated control circuitry.

Additionally, because a given processor in a two or one dimensional array can communicate only with adjacent processors, input and output to the array is considerably restricted and necessarily limited to a predetermined bandwidth which is determined by the number of processors along one edge of the array and the system clock speed.

#### SUMMARY OF THE INVENTION

A multi-dimensional processor array is disclosed for processing data structured in two or more dimensions. Such a multi-dimensional processor array includes a plurality of processor cells interconnected to form an N dimensional array where N is typically three or more dimensions. Each of the processor cells has 2N data signal ports for transmitting and receiving data to and from at least 2N devices.

In a preferred embodiment, the multi-dimensional processor array is configured as a three-dimensional array having defined rows, columns and levels of depth, and in which each processor cell includes six data signal ports operative for transmitting and receiving data to and from up to six dimensionally adjacent processor cells or data

- 3 -

communications devices. The processor cells are arranged in a three-dimensional array forming a first group of processor cells having six dimensionally adjacent processor cells, and a second group of processor cells having fewer than six dimensionally adjacent processor cells. Accordingly, each processor cell in the second group of processor cells includes at least one unconnected or surplus data signal port having the capability for connecting to one communication device such as an input/output device or additional memory. The preferred embodiment further includes at least one input/output device coupled to the surplus data signal ports of the second group of processor cells, for transferring data between the input/output device and the second group of processor cells. A selected number of the processor cells having 2N dimensionally adjacent processor cells each also have at least one data signal port coupled to additional memory or to an input/output device, which, when combined with the surplus data signal ports of the second group of processor cells, provide massively parallel input/output between the multi-dimensional processor array and the input/output device.

Also disclosed is a multi-dimensional processor system, for processing multi-dimensionally structured data. Such a system includes a front end processor, for providing processor array commands in response to application programs running on the front end processor. A processor cell controller, responsive to the processor array commands, provides a sequence of processor cell instructions to all of the processor cells of the multi-dimensional processor array.

In a preferred embodiment, the processor cell controller of the multi-dimensional processor array converts processor array commands received from the front end processor operating as a preprocessor device, into intermediate commands or instruction words called

- 4 -

macro-instructions, while a serializer converts these macro-instructions into a sequence of processor array cell instructions called nanoinstructions.

5

#### DESCRIPTION OF THE DRAWINGS

These and other features of the present invention will be better understood by reading the following detailed description of the invention, taken together with the drawings, wherein:

10

Fig. 1 is an illustration of a three-dimensional 3 x 3 x 4 processor array comprised of 36 processor cells;

Fig. 2 is a partially exploded view of the three-dimensional processor array of Fig. 1;

15

Fig. 3 is a representation of a four-dimensional 3 x 3 x 3 x 3 processor array according to this invention;

Fig. 4 is a block diagram illustrating the internal structure of a processor cell according to this invention; and

20

Fig. 5 is a schematic representation of the multi-dimensional processor system and processor array according to this invention, illustrating the massively parallel input/output feature of the invention.

#### DETAILED DESCRIPTION OF THE INVENTION

25

The multi-dimensional processor array herein disclosed typically includes a multi-dimensional array of three or more dimensions. The three dimensional processor array 10 illustrated in Fig. 1 is a 3 x 3 x 4 array, comprised of (4) four, two dimensional 3 x 3 sub-arrays 15-18 of processor cells 12.

30

35

Each processor cell of the N dimensional array includes 2N data signal ports operative for forming data signal paths for transmitting and receiving data to and from at least 2N adjacent processor cells or data communication devices. In this example, each processor cell 12, shown in Fig. 2, of each sub-array such as

- 5 -

sub-array 16, (shown in an exploded view) includes six data signal ports 20a-20f, which allow each processor cell to send and receive data to and from at least six adjacent processor cells or data communication devices such as input/output devices or extended memory.

Although each processor cell is adapted for transferring data to and from at least six adjacent processor cells or data communication devices, not all processor cells are conceptually positioned adjacent to or interconnected with six processor cells. For example, a number of processor cells such as processor cells 12a are conceptually located on one of the "faces" of the multi-dimensional processor array, and have at least one data signal port 22 which, for a given array configuration, is surplus or whose signal port is ignored. Such surplus signal ports 22 form the basis of the reconfigurable multi-dimensional array disclosed in U.S. Patent Application Number 07/529,962 entitled Dimensionally Reconfigurable Multi-Dimensional Processor Array, filed concurrently herewith assigned to the same assignee as the instant application and incorporated herein by reference.

The multi-dimensional processor array of the present invention is not limited to a three dimensional array. It is a feature of the invention that a multi-dimensional array of N-dimensions may be arranged by providing a plurality of processor cells having  $2N$  data signal ports as illustrated in Fig. 3 wherein is shown four dimensional array 30 comprised of a plurality of three dimensional sub-arrays 32-36. Three dimensional sub-arrays 32-36 may include any number of processor cells 12, each having  $2N$ , or in this example 8, data signal ports. In addition to the 6 data signal ports provided for interconnecting processor cells 12 as a three dimensional sub-array, each processor cell 12 includes two additional data signal ports 20g and 20h. For the purposes of clarity, the other

- 6 -

interconnections between the three dimensional sub-arrays are omitted. The additional data signal ports 20g and 20h allow a given processor cell 12 from one three dimensional sub-array to interconnect with a corresponding processor cell in a dimensionally adjacent three dimensional sub-array, thereby forming a four dimensional array.

The concept of a four dimensional array can be better understood by considering, for example, each processor cell of three dimensional sub-arrays 32-36 as corresponding to a spatial position, with three dimensional sub-array 34 representing spatial data at a given time; three dimensional processor sub-array 32 representing spatial data at a time prior to that of sub-array 34; and finally with three dimensional sub-array 36 representing spatial data at a time after that of sub-array 34. It is therefore apparent that a four dimensional array according to the present invention is capable of solving a four dimensional problem as would be involved in solving equations necessitating the resolving of three dimensional spatial data over a period of time. The present invention is not to be limited to a four dimensional processor array since it is evident that the array may be expanded to N-dimensions by providing additional data signal ports interconnecting corresponding processor cells in any given number of sub-arrays.

The internal structure of each of the processor cells 12 is illustrated in greater detail in Fig. 4. Each processor cell in the preferred embodiment includes a 2,048 bit memory 134, each bit of which is addressable under control of memory address bus 136. The 12 bits of memory address bus 136, of which one bit is currently unused and reserved for expansion, are part of the nanoinstruction received from the system instruction serializer described below.

Each processor cell 12 also includes a one bit memory latch 138 as well as a one bit I register 140, R



- 7 -

register 142, C register 144 and S register 146. I register 140 is an interprocessor communication register and receives a one bit input from input multiplexor 148. Input multiplexor 148 accepts input from six adjacent processor cell outputs 150 in the +X, +Y, +Z, -X, -Y and -Z directions. Additionally, input multiplexor 148 also receives as input processor output 152, as well as flag output 154. Multiplexor 148 outputs one bit to I register 140 as a function of a three bit I Input Code 156. The three bit I Input Code is also a part of the nanoinstruction. Although each nanoinstruction is comprised of 60 bits, only 43 bits go to each processor cell. Definition of the various bits that comprise these 43 bits of the nanoinstruction are represented in Table 1 reproduced below.

Table 1

| Field  | Width |
|--|-------|
| Memory address   | 12    |
| Processor output ALU function  | 8     |
| Flag output ALU function   | 8     |
| I input<br>0: +X                      3: -Y                      6: Processor output<br>1: +Y                      4: -X                      7: Flag output<br>2: +Z                      5: -Z | 3     |
| MRC Code<br>0: Memory latch              1: C              2: R  | 2     |
| IRC Code<br>0: I                      1: C              2: R   | 2     |
| SRC Code<br>0: S                      1: C              2: R   | 2     |
| Write memory enable  | 1     |
| Write I register enable  | 1     |
| Write R register enable  | 1     |
| Write S flag enable  | 1     |
| Write C flag enable  | 1     |
| Ignore S flag  | 1     |

Table 1    Nanoinstruction Fields

- 9 -

As represented in Table 1, the three bit I Input Code selects one of the inputs to input multiplexor 148 as a function of the three I Input Code bits 156. For example, if the I Input Code bits are all set to zero, the +X input to input multiplexor 148 is directed to I register 140. The output from I register 140 is directed to output signal path 158 which is connected to six adjacent processor cells as one of its inputs 150, and to IRC multiplexor 160 which provides one of the inputs to ALU 162.

Writing to the I, R, C and S registers, as well as the memory, is enabled by means of processor control circuitry 164 under control of the appropriate write enable bits and the ignore S flag bit from the nanoinstruction, as well as the S flag.

Each processor cell reads and writes data once during each nanoinstruction cycle. A typical nanoinstruction cycle in the present embodiment is approximately 125 nanoseconds in duration, with a 62.5 nanosecond read phase followed by a 62.5 nanosecond write phase, although any appropriate read and write phase timing period may be employed.

During the first half of each nanoinstruction cycle, each processor cell reads the bit from its memory location specified by the 12-bit memory address given in the nanoinstruction. The bit is read into memory latch 138. Three 3-to-1 multiplexors 160, 166, 168 select three of the five possible input bits under control of the respective multiplexor codes, namely; IRC multiplexor code 170, MRC multiplexor code 172 and SRC multiplexor code 174.

There are five possible input bits to the ALU 162. The five possible input bits include the memory bit from memory latch 138, along with one bit from each of the I, R, C and S internal registers 140-146 respectively. The MRC, IRC and SRC codes also form part of the

- 10 -

nanoinstruction and are identified in the nanoinstruction definition represented in Table 1 above.

ALU 162 accepts three 1-bit inputs, and produces two output bits, namely processor output 152 and flag output 154. To permit each of the ALU output bits to be independently selected by the three input bits, ALU 162 is implemented as two 8-to-1 multiplexors including processor multiplexor 175 and flag multiplexor 177. The three input bits provide a control code for selecting one bit from each multiplexor as illustrated in Table 2 shown below.

Table 2

| Memory Input<br>MRC MUX | Processor Input<br>IRC MUX | Flag Input<br>SRC MUX | ALU Code Bit<br>Position |
|-------------------------|----------------------------|-----------------------|--------------------------|
| 0                       | 0                          | 0                     | 0 - LSB                  |
| 0                       | 0                          | 1                     | 1                        |
| 0                       | 1                          | 0                     | 2                        |
| 0                       | 1                          | 1                     | 3                        |
| 1                       | 0                          | 0                     | 4                        |
| 1                       | 0                          | 1                     | 5                        |
| 1                       | 1                          | 0                     | 6                        |
| 1                       | 1                          | 1                     | 7 - MSB                  |

- 11 -

Eight data bits are supplied to each of ALU multiplexors 175 and 177 by separate 8 bit ALU code fields 176 and 178 of the nanoinstruction. The 8 bit processor ALU code 176 and the flag ALU code 178 are selected to represent the desired function or result of any logical operation performed on one or more of the three multiplexor control bits. For example, if memory data stored in memory latch 138 is to be directed to processor output 152, the two bit MRC code 172 which controls MRC multiplexor 166 would be set to 00, see Table 1. Processor ALU code 176 would then be set to 11110000. With this processor ALU code, a "0" from the memory latch 138 and MRC multiplexor 166 will produce a "0" on processor output 152 regardless of the state of the two remaining inputs to the processor multiplexor. See Table 2. Similarly, a logic "1" from memory latch 138 will produce a logic "1" on processor output 152 regardless of the state of the two remaining input bits to the ALU from the IRC and SRC multiplexors.

Processor output 152 is directed to memory write data multiplexor 180 which selects either memory read data from memory latch 138 or ALU processor output 152, either of which may be written back into memory during the second half or write phase of the nanoinstruction cycle. Control of memory write data multiplexor 180 is accomplished under direction of memory write enable signal 182 and the Ignore S flag signal, both of which are part of the nanoinstruction, as well as by the S register 146. Processor output 152, as well as flag output 154 are directed to I input multiplexor 148. Additionally, the ALU processor output 152 serves as input to R register 142, while flag output 154 is directed as input to C and S registers 144 and 146 respectively.

Fig. 5 illustrates the multi-dimensional processor system 100 of the present invention incorporating a plurality of such processor cells. The system includes an

- 12 -

appropriate front end processor 102 which serves as a command preprocessor interfacing with processor controller 104 by means of an interface such as a small computer system interface (SCSI) 106. In the preferred embodiment, front end processor 102 is a conventional computer operating under control of a Unix<sup>TM</sup> operating system. An example of such a front end processor is a Sun workstation available from Sun Microsystems. Front end preprocessor 102 includes a standard C compiler as well as a preprocessor for the C compiler which allows the system to compile and operate programs written using parallel processing extensions to the C language.

Processor controller 104 provides intermediary processing functions between front end processor 102 and processor array 108. Controller 104 includes control processor 110 which in the preferred embodiment is an AMD-29000 processor. Control processor 110 operates under control of a processor program stored in processor program memory 112. Control processor 110 receives commands to initialize processor array 108, as well as to control input/output transfers between processor array 108, front end processor 102, swapping RAM 116, optional extended swapping ram 134 and optional I/O devices 118. Control processor data memory 114 provides temporary data and processor variable storage to control processor 110.

Front end processor 102 communicates with control processor 110, sending commands to and reading data from the control processor in response to selected commands. Each command normally describes word-oriented unary or binary operations such as ones complement or multiplication. Control processor 110 identifies such commands, and reformats them as a sequence of word-oriented commands called macroinstructions. Macroinstructions are transferred to serializer 120 by initializing registers located within the serializer. Serializer 120 operates under control of microcode stored

- 13 -

in microcode memory 122 and converts each word-oriented macroinstruction into a sequence of bit-oriented commands including processor cell instructions and memory addresses called nanoinstructions which are transmitted to all processors of processor array 108. It is understood that any hardware or software which converts word-oriented to bit-oriented commands may be utilized and is well known to those skilled in the art. An example of such a serializer is illustrated in copending U.S. Patent Application No. 07/529,947 entitled Virtual Processing Instruction and Address Generator for Parallel Processor Array, assigned to the same assignee as the instant invention and incorporated herein by reference. Nanoinstruction memory 124 contains a table of nanoinstruction templates that serializer 120 accesses to form nanoinstructions for the processor array.

The following is an example of a command transfer from the front end processor 102 to control processor 110. By way of illustration, front end processor 102 may send a sequence of 32-bit words for the command "d=e+f" over the small computer system interface 106 to control processor 110. Such a sequence of 32-bit words is illustrated in Table 3 reproduced below.

← 32 bits →

|                      |
|----------------------|
| Code = add e ← f → d |
| d (LSB address)      |
| W(d) = n width of d  |
| e (LSB address)      |
| w(e)                 |
| f (LSB address)      |
| w(f)                 |

Table 3

- 14 -

During the first step of the command transfer, front end processor 102 transmits a 32 bit wide operation code corresponding to the operation "add" to control processor 110. During the second step of the command transfer, the front end processor transmits the memory address of the least significant bit of the parallel variable d. Parallel variables are variables that reside in the same memory location in each processor cell. During the third step of the transfer, the front processor transmits the width or number of bits included in the variable d. Similarly, the fourth through seventh steps of command transfer include transmitting the address of the least significant bit and width of the parallel variables e and f respectively.

From each command, control processor 110 generates one or more macroinstructions which are transmitted to serializer 120. The control processor transmits each macroinstruction to the serializer by initializing registers located within the serializer.

After receiving the macroinstruction, serializer 120 begins generation of the corresponding sequence of nanoinstructions which is broadcast to all of the processor cells in processor array 108.



Table 4

| bits  | 12             | 8               | 8               | 8             | 3           | 2           | 2           | 2       | 1 | 1 | 1 | 1    |
|-------|----------------|-----------------|-----------------|---------------|-------------|-------------|-------------|---------|---|---|---|------|
| Cycle | Mem<br>Address | P<br>ALU<br>MSB | F<br>ALU<br>MSB | Input<br>Code | WRC<br>Code | IPC<br>Code | APC<br>Code | Enables |   |   |   | Ign. |
|       |                |                 |                 |               |             |             |             | MEM     | I | R | S | C    |
| 1     | c              | 1111 0000       | ~               | ~             | m(00)       | ~           | ~           | 0       | 0 | 1 | 0 | 0    |
| 2     | f              | 0011 1100       | 1100 0000       | ~             | ~(00)       | r(10)       | ~           | 0       | 0 | 1 | 0 | 1    |
| 3     | d              | 1111 0000       | ~               | ~             | r(10)       | ~           | ~           | 1       | 0 | 0 | 0 | 0    |
| 4     | 2+1            | 1111 0000       | ~               | ~             | m(00)       | ~           | ~           | 0       | 0 | 1 | 0 | 0    |
| 5     | f+1            | 1001 0110       | 1110 1000       | ~             | m(00)       | r(10)       | c(01)       | 0       | 0 | 1 | 0 | 1    |
| 6     | 1-1            | 1111 0000       | ~               | ~             | r(10)       | ~           | ~           | 1       | 0 | 0 | 0 | 0    |

Note: ~ = don't care

- 16 -

During the first cycle of nanoinstruction generation illustrated in Table 4 above, the object of the nanoinstruction is to move the one bit of data pointed to by memory address e to the R register located within each processor cell. To accomplish this, serializer 120 produces a 16 bit memory address (four bits of which are now unused) corresponding to memory address e which is the address of the least significant bit of data. Next, the serializer produces a processor ALU code which will produce a processor output of "0" if the data stored at memory address e is a logic 0, and a processor output of "1" if the data stored at memory address e is a logic 1. During this cycle, the flag ALU code and the input code are not necessary and will, by definition, be logic zeros. See also Table 2. The next portion of the nanoinstruction is the two bit MRC code 00 which indicates that the MRC multiplexor will select data from the memory latch. Since this cycle is not concerned with data from either the IRC or SRC multiplexors, both the IRC and SRC codes are irrelevant during this cycle. Finally, the R enable is set to indicate that the processor output is to be stored in the R register.

During the second cycle of the nanoinstruction generation wherein a second nanoinstruction is provided, the object of the cycle is to access the data bit stored at the f memory location and add that bit to the previously accessed bit from the e memory location which is now stored in the R register of each processor cell. To accomplish this, serializer 120 provides the memory address f followed by the processor ALU code 00111100. This particular processor ALU code represents that as long as either the R register or the memory latch, but not both, is set to a logic 1, the processor output will be a 1. If neither the R register nor the memory latch are a logic 1, or if both are a logic 1, the processor output will be a logic 0. This corresponds to the possible

- 17 -

results of the addition of two bits. Next, the serializer sets the flag ALU code to 11000000. This indicates that if both the memory latch and the R register are set to 1, the flag output will be set to 1. This will enable the processor to store a carry condition if both bits being added are a logic 1. As in the first cycle, since no input is being received from an adjacent processor cell, the input code is not required. The two bit MRC code is set to 00 to indicate that data from the memory latch is to be read into the MRC multiplexor, while the IRC code is set to 10 to indicate that data from the R register is to be processed through the IRC multiplexor. Finally, the R and C enables are set to indicate that the results of the processor output are to be latched in the R register while the results from the flag output will be latched in the C register to indicate a carry.

The purpose of the third cycle shown in the nanoinstruction sequence of Table 4 is to store the result of the addition of the first two bits located at memory addresses e and f into the memory location at memory address d. Accordingly, the serializer first generates the memory address d and the processor ALU code which directs that the input from the MRC multiplexor will be passed through the processor multiplexor to the processor output. The MRC code is set to 10 indicating that the MRC multiplexor is to select input from the R register. Lastly, the memory enable bit is set so that during the nanoinstruction write phase, the processor output is written into memory address d. This completes the processor cell's half-add of the least significant bits (bit position 0) of a data field that is n bits wide.

The fourth, fifth and sixth cycles of the nanoinstruction sequence perform a full add of the bits located at bit position 1 which are stored at memory addresses e+1 and f+1. During cycle 4, data is read from memory address e+1 and stored in the R register as

- 18 -

described during cycle 1. During cycle 5, the nanoinstruction bit sequence directs each processor cell of the processor array to add the bits located at memory address  $f+1$  to the bit stored in the R register which was derived from memory address  $e+1$  during cycle 4, along with any carry that was generated during the half-add in cycle 2 and stored in the C register. Accordingly, the processor ALU code at cycle 5 is selected to provide a logic 1 on the processor output as long as only one of either the memory bit, the R register bit or the C register bit are set to a logic 1, or if all three bits are set to a logic 1. The flag ALU code, in contrast, is selected such that a logic 1 will be provided on the flag output whenever two or more of the three bits are set to a logic 1, indicating a carry.

The two bit MRC code is set to 00 to indicate input from the memory latch while the IRC code is set at 10 to select input from the R register. The SRC code is set to 01 to select input from the C register. The R enable bit is set to allow processor output to be stored in the R register while the C enable bit is set to allow the carry to be stored in the C register. Finally, cycle 6 is identical to cycle 3 in that it provides a nanoinstruction that directs each processor cell of the processor array to store the contents of the R register which represents the result of adding bit position 1, in a memory location indicated by memory address  $d+1$ .

Cycles 4, 5 and 6 are repeated  $n-2$  more times in order to perform the addition indicated by the command  $d=e+f$  for  $e$  and  $f$  of  $n$  bits in width.

Bi-directional edge FIFO 126 buffers input/output data transfer between control processor 110 and processor array 108. Edge FIFO is so named because it connects to the  $(-X, -Z)$  edge 130 of processor array 108. Since processor array 108 typically has 32 processor cells in the Y dimension, bi-directional edge FIFO 126 is 32 bits

- 19 -

wide, with one bit of the edge FIFO connected to each processor on the (-X, -Z) edge of the array.

5 The multi-dimensional processor system makes use of both parallel variables as well as non-parallel variables, which reside in the front end processor's memory. To load an n-bit parallel variable (where  $n \leq 32$ ) into each of the processor cells of processor array 108, control processor 110 first loads 32 words of 32-bits in length for the processors on the (+X, +Z) edge of the array into edge FIFO 126. Control processor 110 then instructs  
10 serializer 120 to generate a nanoinstruction sequence that loads a 32-bit temporary parallel variable in each processor in the -Z face of the array with a corresponding value from its -X neighbor. Since the processors on (-X, -Z) edge 130 of processor array 108 have no neighbor in the -X direction, each of these edge processors reads data from edge FIFO 126. Note that the temporary variable in each processor cell on the (-X, -Z) edge of the array now  
15 contains 32-bits of the same bit position (for example 32 bits from bit position 0) of data to be loaded into the 32 processors on the (+X, +Z) edge of the array, rather than an N-bit word value.

Control processor 110 then proceeds to load data destined for the processors in each successive -X column  
25 in the +Z plane of the array from the edge FIFO until each temporary parallel variable in every processor in the -Z plane of the array has been loaded with data passed through edge FIFO 126.

Control processor 110 then instructs serializer 120  
30 to produce a nanoinstruction sequence that causes each processor in array 108 to load data from its -Z neighbor. In this manner, data is shifted in the +Z direction and the entire sequence repeats to load data for the processors in each successive plane in the +Z direction  
35 until the temporary variable in every processor in the array has been loaded with data passed through the edge FIFO.

- 20 -

At this point, every data bit that has been loaded into the array resides in the temporary parallel variable in a processor at the X and Z coordinates where it is to be stored. However, most of these data bits are not in the processors at the proper Y coordinates. If the 32 words of the 32-bit temporary variable in each of 32 processor cells in every column is viewed as a 32 x 32 matrix of one bit values, all of the data bits may be moved to the proper Y coordinate by transposing all of these matrices in parallel. The result of this transpose operation is stored directly in the parallel variable that is the destination of the loaded data as the transpose is accomplished.

The control processor 11C reads data from processor array 108 by means of the inverse operation. First, the control processor instructs the serializer to produce a nanoinstruction sequence that causes the data in every processor cell column to be transposed in parallel, leaving the result in a 32-bit temporary parallel variable. Then, it instructs the serializer to produce a nanoinstruction sequence that causes the edge FIFO to be loaded with the 32 values of the temporary parallel variable from the processors on the (-X, -Z) edge of the array, and every processor cell in the -Z plane of the array to load its parallel temporary variable with the corresponding value from its +X neighbor. The control processor then instructs the serializer to repeat this sequence until the processor array has written all values of the temporary parallel variable from the processors in the -Z plane of the array to the edge FIFO. The control processor then instructs the serializer to produce another sequence of nanoinstructions that causes every processor in the array to load its parallel temporary variable with the corresponding value from its +Z neighbor. The control processor repeatedly reads the edge FIFO and instructs the serializer to repeat the nanoinstruction sequence for

- 21 -

reloading it until it has read the parallel variable from all processors in the array.

5           Controller 104 uses processor array 108 in an optimum configuration. For example, if the Z dimension of a given problem space is 1, controller 104 automatically configures processor array 108 as a two dimensional processor array, which provides a larger number of physical processors in the X and Y directions. In this manner, the X and Y dimensions of the problem space can be  
10           enlarged without exceeding the physical capacity of processor array 108.

Processor array 108 is a single instruction, multiple data (SIMD) processor array comprising a plurality of bit serial processor cells 132. Although  
15           individual processor cells 132 each have their own 2,048 bits of local memory, certain types of processing such as solving partial differential equations with finite difference approximations over a large number of nodes or displaying high resolution voxel databases, require a  
20           physical processor cell to produce an amount of intermediate data that is too large to be stored in its own internal memory. Accordingly, swapping RAM 116 provides additional memory to the processor cells. Swapping RAM 116 is generally interfaced with the  
25           processor array 108 through every fourth processor cell plane in the Y direction such as planes 133. During any cycle when the swapping RAM 116 is read, data is shifted four times in the -Y direction from the swapping RAM into each processor cell 132 in each successive Y plane.  
30           Writing data from processor cells 132 to swapping RAM 116 involves the reverse process.

Optional I/O devices 118 include devices such as a video processor and a two dimensional array of sensors such as temperature sensors. Optional I/O devices 118  
35           interface with processor array 108 through every 16th column of processor cells in the X direction such as

- 22 -

plane 136 and the +X plane 138 of the processor array. Interfacing I/O devices 118 with an entire plane of processor array 108 as well as every 16th column of processor cells in the X direction provides very fast (up  
5 to 1 gigabyte/second for an 8 MHz clock) input/output operations between processor array 108 and the optional I/O devices 118. Optional extended swapping RAM 134 may be provided to serve as additional memory to processor array 108. Optional extended swapping RAM 134 also  
10 interfaces with every 16th column of processor cells in the X direction as well as the +X plane of the array (although it appears on the -X side of the array is the figure for purposes of clarity).

15 Modifications and substitutions to the present invention by one of ordinary skill in the art are considered to be within the scope of the present invention and the claims which follow.



- 23 -

CLAIMS

1. A multi-dimensional processor array having three or more dimensions, for processing multi-dimensionally structured data comprising:
  - 5 a plurality of processor cells, interconnected to form an N dimensional array, said N dimensional array having a plurality of N-1 dimensional sub-arrays of said processor cells; and
  - each of said processor cells having 2N data signal ports, for transmitting and receiving data to and from at least 2N devices.
- 10 2. The processor array of claim 1 wherein said 2N devices include at least one processor cell.
- 15 3. The processor array of claim 1 wherein each processor cell includes an interface to permit reception of commands from a processor cell controller.
- 20 4. The processor array of claim 3 wherein said interface includes an arithmetic logic unit operative for receiving and executing commands from said processor cell controller.
- 25 5. The processor array of claim 3 wherein said commands include a memory address.
6. The processor array of claim 5 wherein each processor cell includes memory, responsive to said memory address, for storing and retrieving data.
- 30 7. The processor array of claim 4 further including a preprocessor device for providing processor array instructions in response to application programs running on the preprocessor.

- 24 -

8. The processor array of claim 7 wherein said processor cell controller converts said processor array instructions to one or more intermediate instruction words.

5 9. The processor array of claim 8 further including a processor cell instruction and address generator, for converting said intermediate instruction words into a sequence of processor cell instructions.

10 10. The processor array of claim 9 wherein said processor cell instructions include at least an instruction portion and an address portion.

15 11. The processor array of claim 10 wherein each of said processor cell instructions include a plurality of bits each having a preassigned designation.

20 12. The processor array of claim 11 wherein said preassigned bit designations include processor cell memory address bits and processor cell instruction bits.

25 13. The processor array of claim 10 wherein said arithmetic logic unit is comprised of two 8-to-1 multiplexors.

14. The processor array of claim 13 wherein the output of each of said 8-to-1 multiplexors are selected as a function of three input control signals.

30 15. The processor array of claim 14 wherein the 8 bit input to each of said 8-to-1 multiplexors form part of said processor cell instruction bits.

35 16. The processor array of claim 14 wherein said three input control signals are provided by three 3-to-1 multiplexors.

- 25 -

17. The processor array of claim 16 wherein said three multiplexors are adapted for selecting any combination of at least five input signals.
- 5 18. The processor array of claim 17 wherein said five input signals include input from memory, external devices and the processor cell's arithmetic logic unit.
- 10 19. The processor array of claim 18 wherein said external devices include dimensionally adjacent processor cells or data communications devices.
- 15 20. The processor array of claim 18 wherein a plurality of said five input signals are stored in a corresponding plurality of latches.
21. The processor array of claim 20 wherein said latches are enabled in response to latch enabling circuitry.
- 20 22. The processor array of claim 21 wherein said latch enabling circuitry is responsive to said processor cell instructions.
- 25 23. The processor array of claim 17 wherein the output of each of said three 3-to-1 multiplexors is selected as a function of two input control signals.
- 30 24. The processor array of claim 23 wherein the two input control signals to each of said three multiplexors are provided by said processor cell instructions.
- 35 25. The processor array of claim 1 wherein said plurality of processor cells include a first group of processor cells having  $2N$  dimensionally adjacent processor cells, and a second group of processor cells having fewer than  $2N$  dimensionally adjacent processor cells.

- 26 -

26. The processor array of claim 25 wherein each processor cell from the second group of processor cells include at least one surplus data signal port operative for transmitting and receiving data to and from at least one additional device.

27. The processor array of claim 26 further including at least one device coupled to at least one of said surplus data signal ports, for transferring data between said device and one or more processor cells from said second group of processor cells.

28. The processor array of claim 27 wherein said first group of processor cells having  $2N$  dimensionally adjacent processor cells include one or more of processor cells each having at least one data signal port coupled to said at least one device.

29. The processor array of claim 28 wherein said at least one device includes at least one input/output device.

30. The processor array of claim 28 wherein said at least one device includes at least one memory storage unit.

31. A three-dimensional processor array, for processing multi-dimensionally structured data comprising:

a plurality of processor cells, interconnected to form in a three dimensional array, said three dimensional array having a plurality of two dimensional sub-arrays of processor cells; and

each of said processor cells having six data signal ports operative for forming six data signal paths, for transmitting and receiving data to and from at least six devices.

- 27 -

32. A multi-dimensional processor system, for processing multi-dimensionally structured data comprising:

a multi-dimensional processor cell array, including a plurality of processor cells interconnected to form an N dimensional array, said N dimensional array having a plurality of N-1 dimensional sub-arrays of processor cells; each of said processor cells having 2N data signal ports for transmitting and receiving data to and from at least 2N devices;

a preprocessor device, for providing processor array instructions in response to instructions executed on the preprocessor; and

a processor cell controller, responsive to said processor array instructions, for providing a sequence of processor cell instructions to each of said processor cells of said multi-dimensional processor array.

33. The system of claim 32 wherein said processor cell controller converts said processor array instructions to one or more intermediate instruction words.

34. The system of claim 33 further including a processor cell instruction and address generator, for generating a sequence of processor cell instructions.

35. The system of claim 34 wherein said sequence of processor cell instructions include processor cell memory address bits and processor cell instruction bits.

## AMENDED CLAIMS

[received by the International Bureau  
on 25 October 1991 (25.10.91);

original claims 33-35 cancelled; original claims 1,4,7,9,17,20,  
31 and 32 amended; new claims 33-35 added; other claims unchanged (5 pages)]

1. A multi-dimensional processor array having three or more dimensions, for processing multi-dimensionally structured data comprising:

5 a plurality of processor cells, interconnected to form an N dimensional array having at least three dimensions, said N dimensional array having a plurality of N-1 dimensional sub-arrays of said processor cells; and

each of said processor cells having 2N data signal ports, for transmitting and receiving data to and from 2N dimensionally adjacent devices.

10 2. The processor array of claim 1 wherein said 2N devices include at least one processor cell.

15 3. The processor array of claim 1 wherein each processor cell includes an interface to permit reception of commands from a processor cell controller.

20 4. The processor array of claim 3 wherein said interface includes an arithmetic logic unit operative for receiving and executing processor cell instructions from said processor cell controller.

5. The processor array of claim 3 wherein said commands include a memory address.

25 6. The processor array of claim 5 wherein each processor cell includes memory, responsive to said memory address, for storing and retrieving data.

30 7. The processor array of claim 4 further including a preprocessor device for providing processor array instructions to said processor cell controller in response to application programs running on the preprocessor device.

8. The processor array of claim 7 wherein said processor cell controller converts said processor array instructions to one or more intermediate instruction words.

9. The processor array of claim 8 wherein said processor cell controller further includes a processor cell instruction and address generator, responsive to said intermediate instruction words, for converting said intermediate instruction words into a sequence of processor cell instructions.

10. The processor array of claim 9 wherein said processor cell instructions include at least an instruction portion and an address portion.

11. The processor array of claim 10 wherein each of said processor cell instructions include a plurality of bits each having a preassigned designation.

12. The processor array of claim 11 wherein said preassigned bit designations include processor cell memory address bits and processor cell instruction bits.

13. The processor array of claim 10 wherein said arithmetic logic unit is comprised of two 8-to-1 multiplexors.

14. The processor array of claim 13 wherein the output of each of said 8-to-1 multiplexors are selected as a function of three input control signals.

15. The processor array of claim 14 wherein the 8 bit input to each of said 8-to-1 multiplexors form part of said processor cell instruction bits.

16. The processor array of claim 14 wherein said three input control signals are provided by three 3-to-1 multiplexors.

17. The processor array of claim 16 wherein said three multiplexors are collectively adapted for selecting any combination of at least five input signals.
- 5 18. The processor array of claim 17 wherein said five input signals include input from memory, external devices and the processor cell's arithmetic logic unit.
- 10 19. The processor array of claim 18 wherein said external devices include dimensionally adjacent processor cells or data communications devices.
20. The processor array of claim 18 wherein said five input signals are stored in five single bit latches.
- 15 21. The processor array of claim 20 wherein said latches are enabled in response to latch enabling circuitry.
- 20 22. The processor array of claim 21 wherein said latch enabling circuitry is responsive to said processor cell instructions.
- 25 23. The processor array of claim 17 wherein the output of each of said three 3-to-1 multiplexors is selected as a function of two input control signals.
24. The processor array of claim 23 wherein the two input control signals to each of said three multiplexors are provided by said processor cell instructions.
- 30 25. The processor array of claim 1 wherein said plurality of processor cells include a first group of processor cells having  $2N$  dimensionally adjacent processor cells, and a second group of processor cells having fewer than  $2N$  dimensionally adjacent processor cells.



26. The processor array of claim 25 wherein each processor cell from the second group of processor cells include at least one surplus data signal port operative for transmitting and receiving data to and from at least one additional device.

27. The processor array of claim 26 further including at least one device coupled to at least one of said surplus data signal ports, for transferring data between said device and one or more processor cells from said second group of processor cells.

28. The processor array of claim 27 wherein said first group of processor cells having 2N dimensionally adjacent processor cells include one or more of processor cells each having at least one data signal port coupled to said at least one device.

29. The processor array of claim 28 wherein said at least one device includes at least one input/output device.

30. The processor array of claim 28 wherein said at least one device includes at least one memory storage unit.

31. A three-dimensional processor array, for processing multi-dimensionally structured data comprising:

a plurality of processor cells, interconnected to form in a three dimensional array, said three dimensional array having a plurality of two dimensional sub-arrays of processor cells; and

each of said processor cells having six data signal ports operative for forming six data signal paths, for transmitting and receiving data to and from up to six dimensionally adjacent devices.

32. A multi-dimensional processor system, for processing multi-dimensionally structured data comprising:

a multi-dimensional processor cell array, including a plurality of processor cells interconnected to form an N dimensional array, said N dimensional array having a plurality of N-1 dimensional sub-arrays of processor cells;

5 each of said processor cells having 2N data signal ports for transmitting and receiving data to and from up to 2N devices;

a preprocessor device, for providing processor array instructions in response to applications programs executed on the preprocessor; and

10 a processor cell controller, responsive to said processor array instructions, for converting said processor array instructions into one or more intermediate instruction words, said processor cell controller further including a processor cell instruction and address generator, responsive to said intermediate instruction words, for converting said intermediate instruction words into a sequence of processor cell instructions provided to each of said processor cells of said multi-dimensional processor array.

20 33. The processor array of claim 1 wherein each of said processor cells includes one data signal input element, for receiving data from said up to 2N devices.

25 34. The processor array of claim 33 wherein said one data signal input element is comprised of one multiplexor having at least 2N inputs, for receiving input data from 2N dimensionally adjacent devices.

30 35. The processor array of claim 35 wherein said one data signal input multiplexor of each of said processor cells includes  $2N + 2$  inputs, for receiving input data from 2N dimensionally adjacent devices, and for receiving two input data signals from an arithmetic logic unit disposed within a respective processor cell.

35

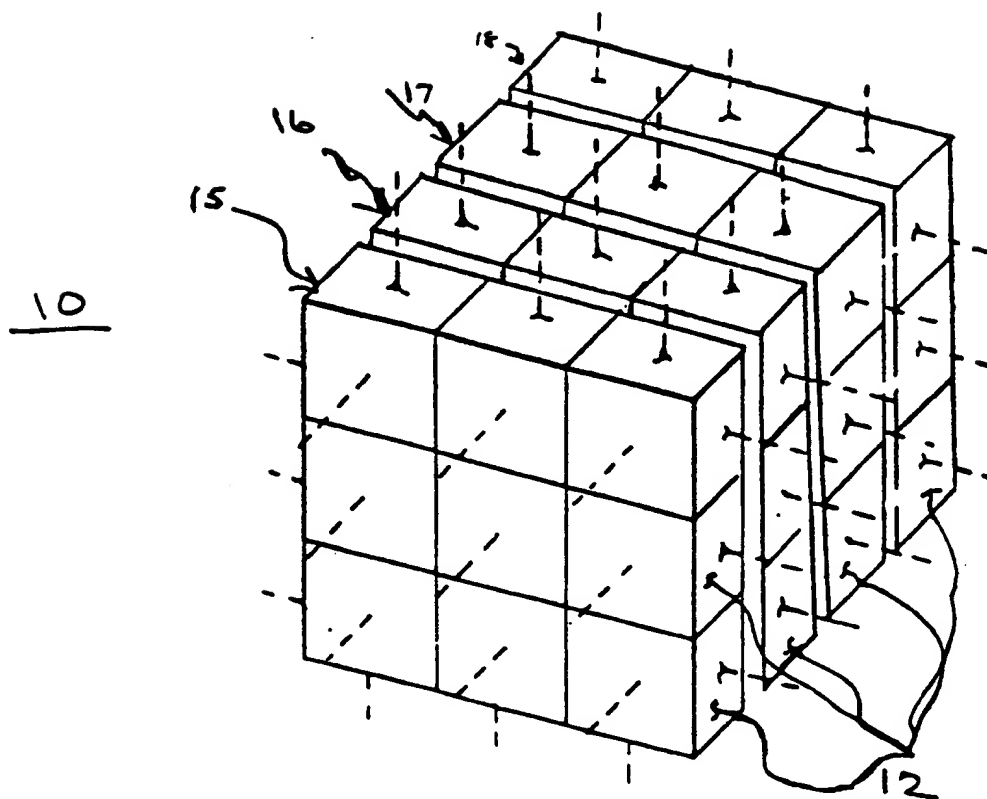


FIG. 1

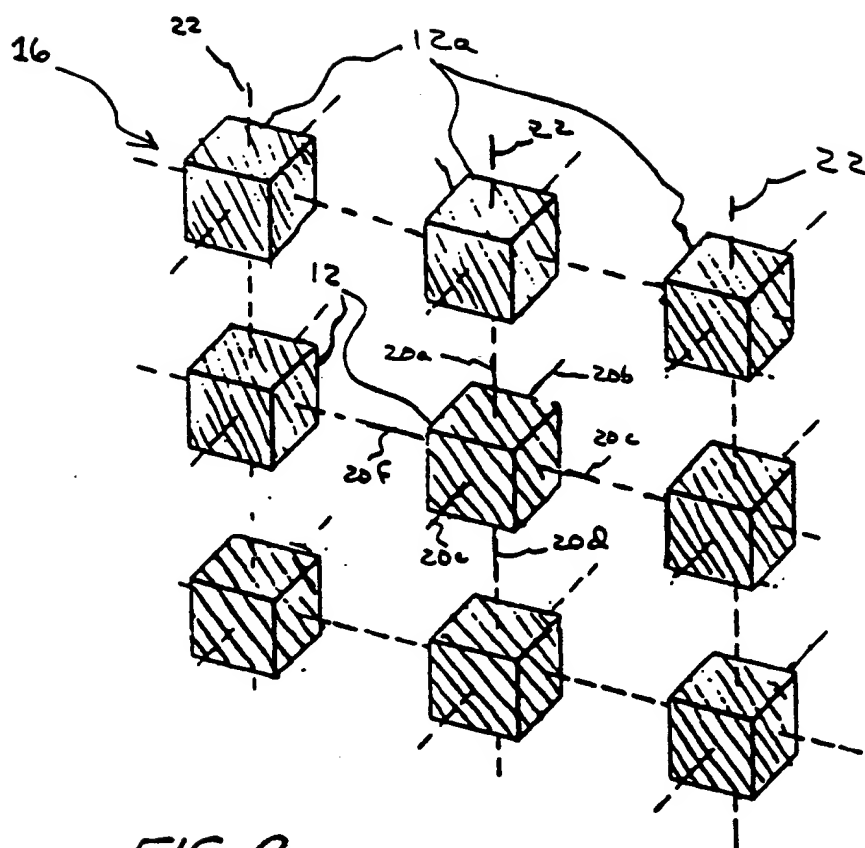


FIG. 2

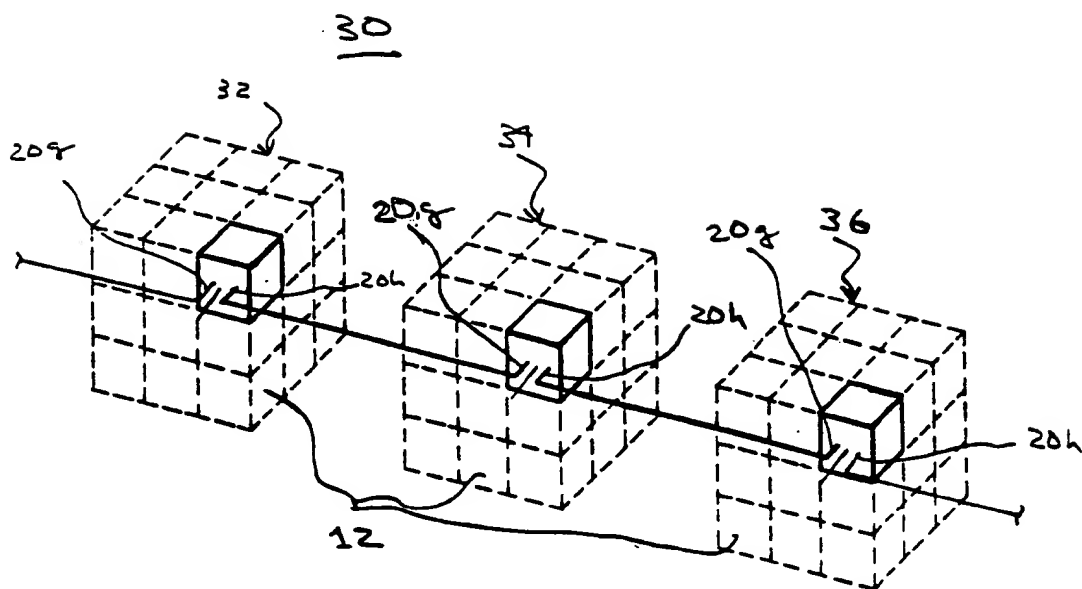


FIG. 3

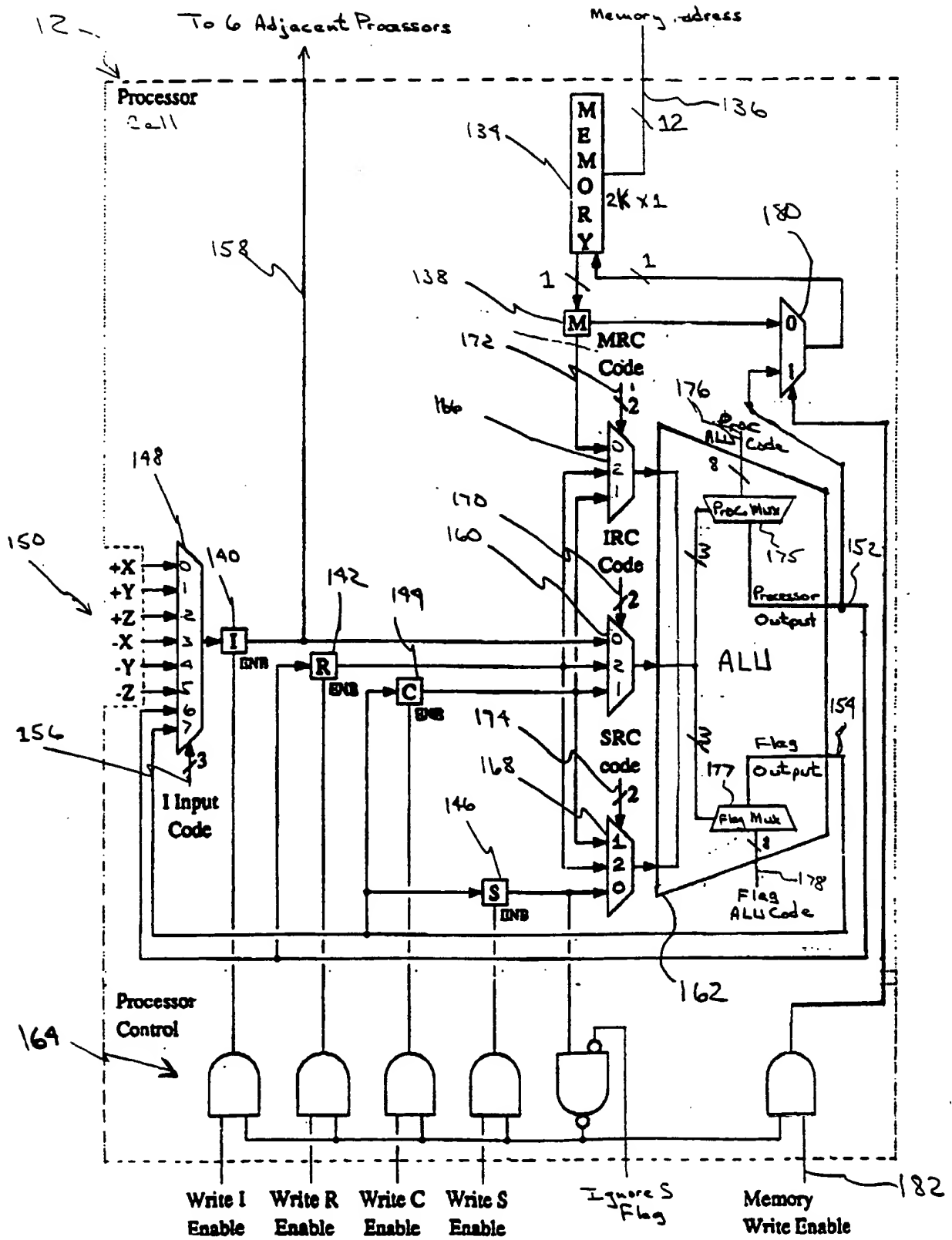


Fig. A

100

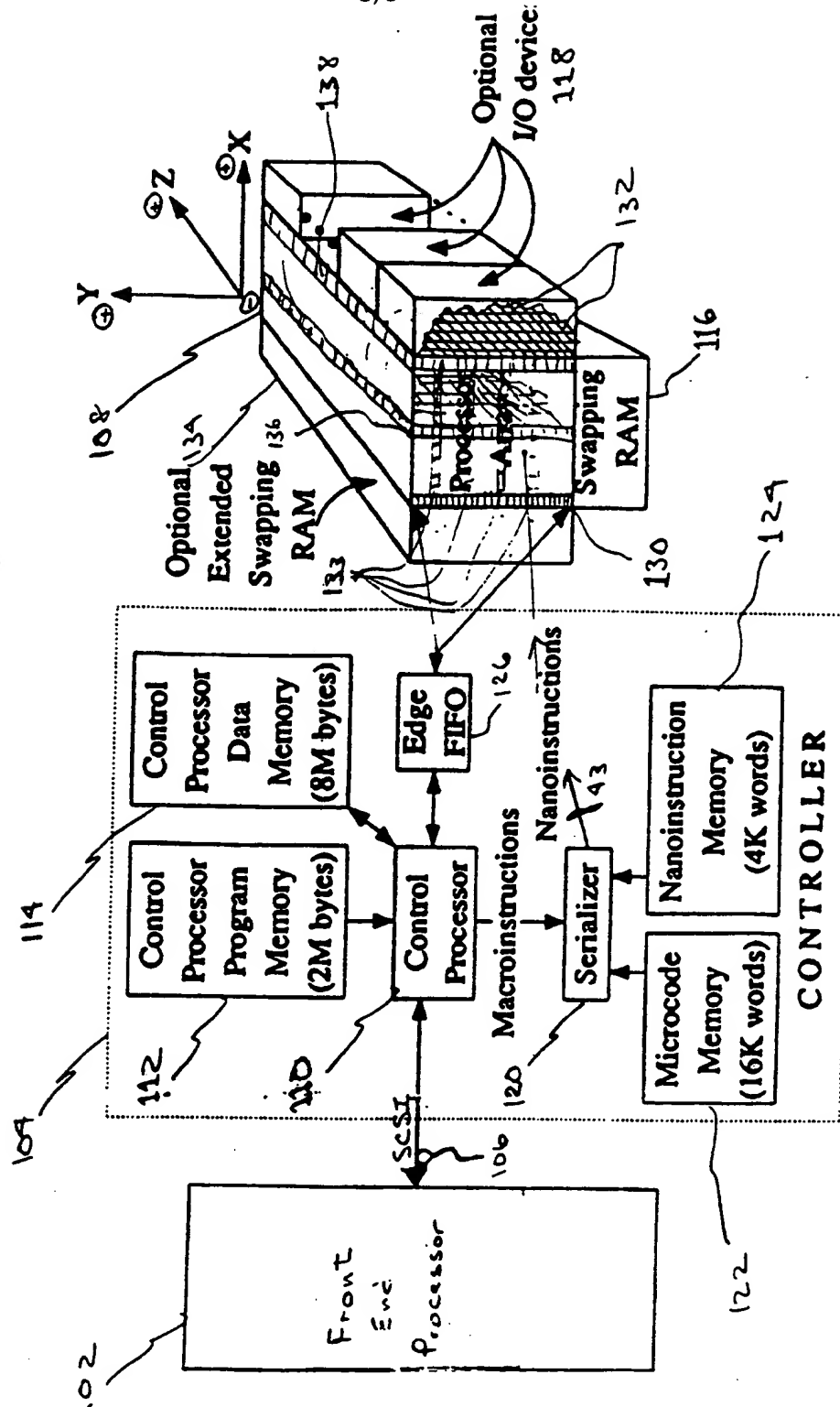
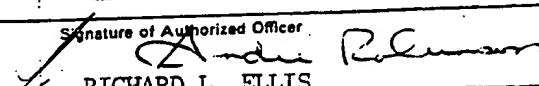


Fig. 5

# INTERNATIONAL SEARCH REPORT

International Application No.

PCT/US91/03347

|   |   |   |
|---|---|---|
| <b>I. CLASSIFICATION OF SUBJECT MATTER</b> (if several classification symbols apply, indicate all) <sup>6</sup>   |   |   |
| According to International Patent Classification (IPC) or to both National Classification and IPC   |   |   |
| IPC(5): G06F 15/80  |   |   |
| US CL.: 364/200, 364/900  |   |   |
| <b>II. FIELDS SEARCHED</b>  |   |   |
| Minimum Documentation Searched <sup>7</sup>   |   |   |
| Classification System   | Classification Symbols  |   |
| US  | 364/200,900 M.S. File   |   |
| Documentation Searched other than Minimum Documentation<br>to the Extent that such Documents are Included in the Fields Searched <sup>8</sup>   |   |   |
| <b>III. DOCUMENTS CONSIDERED TO BE RELEVANT</b> <sup>9</sup>  |   |   |
| Category <sup>*</sup>   | Citation of Document, <sup>11</sup> with indication, where appropriate, of the relevant passages <sup>12</sup>                              | Relevant to Claim No. <sup>13</sup>   |
| Y   | US, A, 4,739,474 (HOLSZTYNSKI) 19 April 1988<br>See figs. 1 and 5, col. 3 lines 38-46, col. 4 lines 21-25 and 33-44 and col. 5 lines 15-19. | 1-35  |
| Y   | US, A, 4,247,892 (LAWRENCE) 27 January 1981<br>See col. 8 line 7 to col. 9 line 9.  | 1-35  |
| A   | US, A, 3,537,074 (STOKES) 27 October 1970   |   |
| A   | US, A, 3,815,095 (WESTER) 04 June 1974  |   |
| A   | US, A, 3,815,097 (GARDNER) 04 June 1974   |   |
| A   | US, A, 3,979,728 (REDDAWAY) 07 September 1976   |   |
| A   | US, A, 3,970,993 (FINNILA) 20 July 1976   |   |
| A   | US, A, 4,580,215 (MORTON) 01 April 1986   |   |
| A   | US, A, 4,720,780 (DOLECEK) 19 January 1988  |   |
| A   | US, A, 4,739,476 (FIDUCCIA) 19 April 1988   |   |
| <div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p><sup>*</sup> Special categories of cited documents: <sup>10</sup></p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> </div> <div style="width: 45%;"> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>"d" document member of the same patent family</p> </div> </div> |   |   |
| <b>IV. CERTIFICATION</b>  |   |   |
| Date of the Actual Completion of the International Search   |   | Date of Mailing of this International Search Report   |
| 12 AUGUST 1991  |   | <b>26 SEP 1991.</b>   |
| International Searching Authority   |   | Signature of Authorized Officer   |
| ISA/US  |   | <br><b>RICHARD L. ELLIS</b> |



## FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

|      |  |
|------|--|
| A, P | US, A, 4, 942, 517 (COK) 17 JULY 1990        |
| A, P | US, A, 4, 992, 933 (TAYLOR) 12 FEBRUARY 1991 |

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE<sup>1</sup>

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers \_\_\_\_\_, because they relate to subject matter<sup>12</sup> not required to be searched by this Authority, namely:
  
2. ☐ Claim numbers \_\_\_\_\_, because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out<sup>13</sup>, specifically:
  
3. ☐ Claim numbers \_\_\_\_\_, because they are dependent claims not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING<sup>2</sup>

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.
2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:
3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:
4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

## Remark on Protest

- ☐ The additional search fees were accompanied by applicant's protest.  
☐ No protest accompanied the payment of additional search fees.